Avionics System Reference Architecture (ASRA),

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What is SAVOIR?

**SAVOIR** means *Space Avionics Open Interface aRchitecture.*

It is an initiative to federate the space avionics community and to work together in order to improve the way that the European Space community builds avionics subsystems.

**SAVOIR** is coordinated by the Savoir Advisory Group including representative of ESA, CNES, DLR, AirbusDS, Thales, OHB, RUAG, Selex, Terma.
SAVOIR mission

- Improve the way we deliver Space Systems (risk & schedule, and therefore cost, and industry competitiveness) by

  An agreed Reference Architecture

  Functional Specifications (OBC, RTU, ...)

  Pre-developed/to be developed Building Blocks

  - If, in ITTs, Customers use agreed mission specification and System Integrators use agreed product specification, then Suppliers should be in a position to have product lines, and System Integrators should have easier integration phases

  Standardized Interfaces
Mission domains considered

- Science and Earth Observation missions with up to 12 years duration to:
  - LEO
  - GEO
  - Lagrange points
  - Interplanetary space
- Telecom missions with up to 15 years lifetime
- The excluded missions are:
  - Manned missions
  - Launchers
- There is however nothing that prevents the Savoir concept and “products” from being used in these missions if the special needs can be somehow fulfilled.
Objectives of the ASRA contract

- The aim of ASRA (Avionics System Reference Architecture, ESA contract) is to define an avionics reference architecture meeting the needs of the various mission domains. Commonality between the solutions recommended for each domain will be maximised whenever possible.

- First work package scope was to agree on a common functional architecture and outline the main functions per functional block. **Functional Reference Architecture** (presented at ADCSS2011)

- Four subsequent work packages for generating:
  1. Ground to Space interfacing, general recommendations
  2. **Generic OBC specification** (presented at ADCSS2012)
  3. **Generic RTU specification**
  4. Platform/Payload interfacing, general recommendations

- Documents 2. and 3. reviewed by ESA and SAG industries

- Update of Functional architecture, OBC Spec and RTU operability
Reference Functional Architecture
Avionics architecture
Some of the variabilities

- X-strap in harness
- X-strap in OBC
- A mix
- RS-422 or LVDS or bilevel

- 5V, 16 V or 28 V
- 10, 180 or 500 mA

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System
alarms

PacketWire

SpaceWire

1553

CPDU

OBC
Trx

"Discrete"
I/O system

P/F

unit

P/L

unit

P/L

unit

P/L

unit

- Analog
- Digital
- Qty from 8 to 36
- Internal or external x-strap

- SpaceWire
- 2 – 12 links
- X-strap in harness
- No x-strap
- No standard protocol

- 28V unreg. power
- 28V reg. power
- 50V "semi" reg power
- 1 ms, 50 ms or 5 s power dropouts

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- 4 – 16 links

1, 2 or 3 buses

CAN

1553 or SpaceWire

- ECSS-E-50-14 with variations
- UARTs (from 2 to 15 lines)
- SDLC/HDLC protocol
- Serial 16 bit
- Serial 32-bit

- 5V, 16 V or 28 V
- 10, 180 or 500 mA
GeSOR: Generic Specification for OBCs and RTUs

OBC & RTU
Generic Spec’s
Definition of Core Functions
They can include:
- Performances,
- Interfaces,
- Applicable docs
TDAs will be activated,
Composed by chapters (modular structure), Living Docs,

Spec’s will allow Competing implementations

Projects SRDs
Tailoring /Addition

Lessons learnt, Clean-up of reqs

Procurement Activity

OBC/RTU BB #1

Adaptation, Qualification

OBC/RTU Reduction of Cost & development time, Flawless process

Lower level BBs

Product lines, Validation

SAG

Standards

Harmo dossier, roadmaps

Iterative process
Produced Documents

SAVOIR Functional Reference Architecture

SAVOIR RTU – Operability Requirements
Avionics functions mapped on units

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OBC Generic Specification

- OBC Spec TOC:
  - **Functional Requirements**
    - Telecommand reception, authentication, decoding and handling.
    - Telemetry Transfer Frame generation, coding and modulation.
    - Processing capability
    - Timing and Synchronisation management.
    - Platform Data Storage
    - Fault Detection Isolation and Recovery (FDIR): Reconfiguration Module (RM), Essential TC function, and a Safeguard Memory (SGM)
    - Security Function (optional)
    - Essential TM (optional)
  - **Interface Requirements**
    - Section with a list of suggested CDMS/CDMU (and a list of non desiderata !!!) requirements for System Requirement Docs
  
Important: Modular Structure [parameters ranges, options are present!]
There are interface requirements in the OBC spec:

- **Requirement Number : SAVOIR.OBC.TC.90**

  **TC Decoder input electrical characteristics.**

  The electrical characteristics of the TC Decoder inputs shall be of Serial Digital Interface (SDI) type.

  (Note SDI ANSI/TIA/EIA-422 is defined in section 8.8 of ECSS-ST-50-14C)

**6.9.1 Mission Data Link Function - PM**

- **Requirement Number : SAVOIR.OBC.MDL.10**

  **No of Processing SpaceWire link interfaces**

  - The OBC shall provide at least four external SpaceWire link interfaces operated two and two in cold redundancy.

  - **Requirement Rationale :** Allows connection to a redundant Payload Data Routing
FDIR requirements in the OBC generic spec

Several requirements address FDIR in term of architecture, redundancy and X-strapping, examples:

- **Requirement Number : SAVOIR.OBC.RM.30**

**RM Task**

The RM shall handle FDIR level 3 and level 4 failures by monitoring alarms from the processing unit as well as a number of system alarms.

*Level 3 is defined as software independent monitoring of the software and processor (OBC internal).*

*Level 4 is defined as software independent monitoring of critical/vital system functions (external to the OBC)*

- **Requirement Number : SAVOIR.OBC.RM.70**

**RM Configuration Interface**

*Each RM shall have a communication path to the Active PM.*

*Requirement Rationale : This link is used to configure and read the status of the RM*
Design requirements in the OBC generic specification

- There are also design requirements in the OBC spec:
  - **Requirement Number : SAVOIR.OBC.TC.100**
    
    **TC Decoder input configuration**
    
    Each TC Decoder shall receive serial telecommand data on three inputs, of which one is dedicated to the EGSE. There shall not be any internal cross-strapping between the two TC Decoders.
  
  - **Requirement Number : SAVOIR.OBC.PM.480**
    
    **Software Storage Memory write protection status in Essential TM**
    
    The write protection status of the Software Storage Memory of both PMs shall be available to the Essential TM
    
    OptionInfo : Option HPTM=Yes
  
  - **Requirement Number : SAVOIR.OBC.PM.485 Data Integrity**
    
    The existence of transmission error protection mechanisms shall be demonstrated for critical links inside the OBC
    
    (e.g. inter processor and inter modules, in particular for the TM/TC channels)
Example of Reqs for SRD in the OBC spec

9.1 Telecommand

SRD.TC.1

It shall not be possible to power off or disable the telecommand function and the Essential TC function by ground command or main processor software.

9.4 Satellite Level Design and Performance Requirements Applicable to the Data Handling Subsystem

SRD.DES.1

The DHS autonomously start the mission software depending on the current spacecraft mode and previous failure history.

Justification: The remaining part of the autonomous spacecraft power-up is assumed to be performed by the ASW

SRD.DES.2

The DHS shall report the results of the mission software boot process via telemetry and to the mission software.
LIST OF NON DESIRABLE SRD REQUIREMENTS

Read errors on PROM and EEPROM shall automatically cause a retry on the redundant bank.

Justification: This is a very detailed implementation requirement which is already covered by the reliability and availability requirements.

The volatile memory shall be protected by an Error Detection and Correction (EDAC) function. This shall allow correcting single bit errors and detecting double bit errors.

Justification: The EDAC algorithm to be used depends on the type of memory selected and the corresponding error modes. Some memories may require other EDAC schemes like multiple bit correction and no double bit error detection.
SAVOIR Functional Reference Architecture is evolving!

- The SAVOIR Functional Reference Architecture and the OBC and RTU generic spec are in continuous evolution
- At the ADCSS2012 day on Mass Memories for Payload applications and file based operations, the CCSDS File Delivery Protocol (CFDP, www.ccsds.org) has been presented and discussed as solution for future Mass Memories.
- CFDP provides the capability to transfer ‘files’ and the associated ‘Meta data’ to and from a spacecraft mass memory [note: the content of the files may be anything: timeline update, ASW image or a SAR image]
- Transmission of massive amount of data on K-band with high data rate and need of retransmission capability can found in CFDP a solution covered by an international standard
- CFDP is baseline in Euclid and in Juice
Various possible options for a CFPD implementation on board have been presented:

- **CFDP entity is located in the SSMM** (for P/L data) but could also be located in the OBC MM (ASW image,...)

- **Direct link from the SSMM to the Transponder** (X, Ka band)

- **CFDP Metadata (CCSDS packet)** for CFDP transactions to/from SSMM are routed directly to SSMM (3) or passed via the OBC (2), see next slides

- **In some on-going project (Bepi Colombo)** implementation of large data transfer are using PUS packet (1)
CFDP Metadata sent through the OBC option 2
CFDP Metadata sent directly to the SSMM option 3
SAVOIR – CDMS Requirements (1 of 2)

Examples

Functional Requirements

- **Requirement Number**: SAVOIR.OBC.CFDP.10
  The exchange of files between the Mass Memory and ground shall follow the CFDP protocol specified in [AD1]

- **Requirement Number**: SAVOIR.OBC.CFDP.20
  The source and destination of files on board will be a location within the Mass Memory

- **Requirement Number**: SAVOIR.OBC.CFDP.30
  The Mass Memory shall allow the on-board storage of:
  - telemetry data (both instruments and CDMS)
  - Scientific data
  - SW images
  - SW patches
  - OBCPs
  To be completed

- **Requirement Number**: SAVOIR.OBC.CFDP.40
  The Mass Memory shall store in each open file the continuous stream of data coming from the associated input port starting after the open command for the file and until the close command for the file is received, or until the max file size limit is reached.
Functional Requirements

- **Requirement Number**: SAVOIR.OBC.CFDP.50
  Mass Memory content shall be maintained across platform re-configuration

- **Requirement Number**: SAVOIR.OBC.CFDP.70
  The Mass Memory shall host a CFDP protocol entity.

- **Requirement Number**: SAVOIR.OBC.CFDP.40
  The Mass Memory shall provide full observability of the status value of the file system

- **Requirement Number**: SAVOIR.OBC.CFDP.40
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- **Requirement Number**: SAVOIR.OBC.CFDP.40
  The Mass Memory shall discard data received over any of its input for which a file is not open.
RUAG Single Board Computer Core (SBCC): a product derived from OBC spec

- KO on 04/07/2012, SRR concluded 21/12/2012, PDR concluded on 05/03/2013, DDR September 2013, activity closure April 2014 (Phase 1)

- 3-phased activity:
  - **Phase 1**: Single Board Computer analysis and design
    - Currently running, expected completion Apr-2014
    - 18 months duration, Target TRL = 4
    - SBC analysis, design and implementation
    - SBC integration with NGMP
    - Development of prototype SW drivers
  - **Phase 2**: FPGA Validation activity
  - **Phase 3**: Single Board Core EQM
RTU/RIU: is it possible to define one single concept for its operability?

- At SAVOIR meeting in June 2013 a decision has been taken: ESA to propose a set of reqs for RTU operability. SAG Industries to comment it.
RTU operability requirements

Requirement Number : SAVOIR.RTU.FU.10 RTU Function 1
The RTU shall perform the following functions:

- Reception and decoding of commands from the OBC on the Command and Control bus
- Generation of data messages to the OBC on the Command and Control bus

Requirement Rationale : The RTU shall be a slave unit controlled by OBC/SMU.

Requirement Number : SAVOIR.RTU.FU.20 RTU Function 2
Besides the functions defined by SAVOIR.RTU.FU.10 the RTU shall perform additional functions as :

- Conditioning and analogue-to-digital conversion of discrete analogue (voltages, currents, thermistor/thermocouples values, ...)
- Acquisition of status signals (relay status and bi-level digital signals)
- ...

Requirement Number : SAVOIR.RTU.FU.30 RTU Function 3
Powering On/Off of the functions listed in SAVOIR.RTU.FU.20 shall be performed under control of the OBC (with exception of ...
RTU functions

- Remote control I/F
- RTU controller
- Data Concentrator:
  Collects data from sensors with standard interfaces
  - Analog
  - Digital bilevel
  - Serial communication like UART and CAN
    Possible future I/F here could be I²C or SPI
- Discrete pulse command interface
- AOCS sensor/actuator interface
- Propulsion interface
- Secondary power distribution to sensors/actuators
- Heaters power distribution
- SpaceWire router
  (in case there is a platform C&C network that needs routing)
- Sync signal distribution (extension of OBC capability)
Conclusions and Future

- **Produced Docs:**
  - Issue 1- draft of Reference Functional Architecture
  - Issue 1- draft of OBC Generic Spec
  - Preliminary version of RTU operability requirements doc

- **On-going & future activities:**
  - SAVOIR Reference Functional Architecture, OBC Generic Spec have been updated by SAG industries
  - Finalization of RTU Operability requirements doc
  - the first two ASRA documents (Reference Functional Architecture and OBC generic spec) will enter in a public review using the European Cooperation for Space Standardization (ECSS) infrastructure (2Q 2014)
  - Future dissemination process controlled by ESA:
    - ESA SRDs / OIRDs inspired by the ASRA work
    - Products to be derived from Savoir concept and Specs
Contact

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Questions?