NASA Data Standards Working Group
CCSDS Spring Meeting - Washington DC - Mar. 10-14, 2008
Space Link Coding & Synchronization

Progress on LDPC Codes at JPL

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TECHNICAL PROGRESS

Summary

- Performed ESTL II tests (Nov. 07) confirming LDPC performance (including frame sync and randomizer)
- Measured (by SW simulation) the performance loss of the AR4JA (2048,1024) LDPC code when the receiver can provide only hard decoded symbols (e.g., the Integrated Receiver)
- Performed a detailed study of the LDPC decoder sensitivity to soft symbol scaling errors (SNR estimation). Investigated several feasible solutions
- Implemented advanced frame synchronizing algorithms and modified them for low-complexity implementation. Measured coding&sync performance, compared to that of existing schemes
- Performed LDPC Decoder Tests at ESTL (JSC) with the Integrated Receiver
- Provided/licensed the JPL-designed FPGA LDPC decoder to industry, NASA centers, and other agencies
- Infusion activities:
  - Low-Density Parity-Check (LDPC) code was chosen for all coded links of Constellation
  - The LDPC code was tested for Space Network (SN) compatibility and performance
  - Mars Science Lab (MSL) to Mars Reconnaissance Orbiter (MRO) link will use same code
  - TDRS K-Band Upgrade Project (TKUP-A)
  - Several new users of JPL LDPC technology
- Participated in the Space Planning Working Group (SPWG, formerly SCAWG) Coding, Modulation, and Link Protocol (CMLP) study
- Contributed to the study on the comparison of the LDPC C2 code and a TPC (Turbo Product Code) – C2 code has better error floor
- Provided clarifications for implementation of de-randomizer
- Study on LDPC on RFI channel
- Performance/complexity measure of non-binary LDPC code
Objectives of this Meeting

• NASA has requested CCSDS to consider the following action:

  “the current CCSDS Experimental (Orange Book) specification CCSDS 131.1-0-2, "Low Density Parity Check Codes for Use in Near-Earth and Deep Space" should be transferred intact onto the Standards Track as a Red Book, with a view to its eventual adoption as a CCSDS Recommended Standard (Blue Book).” [Mike Kearney]

  • This is very important to establish cross-support for the Constellation Program and for future mission planning
  • NASA Orange Book material can be inserted as a new chapter in existing coding Blue Book

• Application Profiles should provide a motivation/rationale for proceeding with standardization of the NASA code set, plus an additional coded modulation scheme as proposed by CNES or ESA

• Discuss charter extension for Coding & Sync WG, and approval. (See text provided at Fall Mtg.)

• Review JPL progress on LDPC codes
Thoughts on Application Profiles

• Three proposed recommendations on the table (Orange Books): NASA, CNES, ESA
• Defining separate application profiles, may lead to a final resolution on a standard, providing solutions for each application profile
• “Conventional” application profiles based on discriminators such as supportable data rate (complexity), latency, bandwidth/power efficiency, range (Near-Earth, Lunar, Deep-Space, etc.), may not provide a clear distinction among the proposed solutions (Which are all excellent, but with very different characteristics)

Profile #1
• Links requiring quick dynamic adaptation to the state of the channel
• Typically requiring a sizable suite of codes and modulations, to provide fine granularity in adapting to channel, and optimizing use of resources and quality of service
• Short round-trip delay required for adaptation (short range), but ARQ not always possible because of broadcast service
• High operational complexity, unless fully automated
• Typically used at high data rates. Long block sizes are suitable. No latency issues

Profile #2
• Links requiring simplicity in operations, where fine granularity dynamic adaptation is not possible. Some adaptation done only on a priori predicts.
• Only a few codes required. No tight integration with matching modulation required
• Low latency may be desired -> shorter block sizes must be provided
Thoughts on Application Profiles

• Profile #1 can be better serviced by the ESA or CNES proposal
  • The CNES proposal would be preferable - maturity of hardware, already an ETSI standard

• Profile #2 can be better serviced by the NASA proposal
  • Being implemented by the Constellation Program, and needing cross-support
  • One could argue that a subset of the CNES proposal may provide also a suitable solution. However, shorter block sizes with no error floors may not be possible due to penalty of short BCHs
• LDPC codes will use existing 64-bit ASM as specified in the NASA Orange Book. (There is an open question on ASM for the rate 7/8 code. Reference to “embedded data stream" marker)
  • The rationale behind this is that 64-bits is enough for reliable synchronization at rate 1/2, and as the code rate approaches 1, as few as 32 symbols could be used. But the savings from using these slightly shorter sync markers isn't worth the additional cost of implementing all the different frame synchronizers.

Note that for turbo codes, which include lower code rates, longer ASMs are needed and recommended
  Rate 1/2; ASM = 2*32bits = 64 symbols
  Rate 1/3; ASM = 3*32bits = 96 symbols
  Rate 1/4; ASM = 4*32bits = 128 symbols
  Rate 1/6; ASM = 6*32bits = 196 symbols
Upcoming SpaceOps 2008 presentation:

Design and Standardization of Low-Density Parity-Check Codes for Space Applications

Kenneth Andrews, Dariush Divsalar, Sam Dolinar, Jon Hamkins, Fabrizio Pollara
Jet Propulsion Laboratory

In the last decade, a family of 16 low-rate turbo codes were designed and standardized, and ground decoders were built for each of the three ground complexes of the Deep Space Network (DSN). These codes are now flying on several missions, including MRO, Messenger, and Stereo. A brief summary will be presented of the turbo code family, along with a performance and complexity comparison to NASA’s legacy codes, and lessons learned.

In the last few years, exciting research developments have produced ten higher rate low-density parity-check (LDPC) codes for the high-data-rate missions anticipated in the coming decades. Originally invented by R. Gallager in his PhD thesis in 1961, this coding technique was largely forgotten for more than 30 years. The primary advance in LDPC codes is the discovery of an iterative decoding algorithm, now called Belief Propagation (BP) decoding, which offers near-optimum performance for large linear LDPC codes at a manageable complexity. The performance
Test and Infusion Activities - LDPC Codes

• Low-Density Parity-Check (LDPC) code was chosen for all coded links of Constellation
  • Constellation FEC trade study, 2006:
    - Recommends AR4JA (2048,1024) LDPC code for all Constellation links
    - On nominal link (initially 72Kbps, reduced to 40Kbps), LDPC codes simplify requirements on antenna design, reducing costs by $6 million.
  • CMLP trade study, 2007:
    - Recommends AR4JA (2048,1024) LDPC code for future missions
• LDPC codes were tested for Space Network (SN) compatibility and performance - ESTL tests, November 2007
  • Performed laboratory tests of new LDPC codes, and compared to existing RS+CC codes
  • Measured improvements of up to 2.4 dB, with decreased latency as well. This gain is even bigger than anticipated because existing RS+CC system is not well implemented
• Infusion (current TRL=6):
  • Mars Science Lab (MSL) - LDPC decoder will fly on MSL (launch 9/2009), and encoder will be programmed into Electra radio on Mars Reconnaissance Orbiter (MRO)
  • Constellation: TSUP contractors implementing LDPC decoder; TKUP contractors implemented LDPC decoder and testing is currently underway at White Sands
  • AOFDM-LDPC system for the Air Force

Many corporations and NASA centers are using the JPL designed FPGA LDPC decoders

Companies
• Efficient Channel Coding (ECC)
• RTLogic
• Avtec
• L3 Communications
• Lockheed Martin
• Cincinnati Electronics
• MIT-LL

NASA centers
• Johnson Space Center
• Goddard Space Flight Center
• Several JPL projects

Spacecraft
• MSL - MRO Proximity Link
• Constellation (baseline plan)
• Cibola Flight Experiment
• AIRSAR (aircraft based)
### Designs for LDPC decoders on FPGA

<table>
<thead>
<tr>
<th>Key:</th>
<th>Code</th>
<th>rate = k/n</th>
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<table>
<thead>
<tr>
<th>AR4JA</th>
<th>rate 1/2</th>
<th>rate 2/3</th>
<th>rate 4/5</th>
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<tr>
<td></td>
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</table>

| k=1024 | 32,64/16=80 Mbps, 160 Msp s 49% logic, 17% RAM | 32,48/10=128 Mbps, 192 Msp s 33% logic, 35% RAM | 32,40/7=183 Mbps, 229 Mps 32% logic, 58% RAM |
|        | 16,32/16=40 Mbps, 80 Mps 23% logic, 17% RAM |                                           |                                           |

| k=4096 | 32,64/26=49 Mbps, 98 Mps 49% logic, 27% RAM | 32,48/18=71 Mbps, 107 Mps 33% logic, 35% RAM | 32,40/13=98 Mbps, 123 Mps 32% logic, 58% RAM |
|        | 16,32/26=25 Mbps, 49 Mps 24% logic, 27% RAM |                                           |                                           |

| k=16384 | 32,64/45=28 Mbps, 57 Mps 49% logic, 45% RAM | 32,48/41=31 Mbps, 47 Mps 33% logic, 35% RAM | 32,40/21=61 Mbps, 76 Mps 32% logic, 58% RAM |
|         | 16,32/45=14 Mbps, 28 Mps 25% logic, 45% RAM |                                           |                                           |

| C2     | rate 0.87451                |                                           |                                           |
| k=7136 | 14,16/7.4=76 Mbps, 86 Mps 16% logic, 24% RAM |                                           |                                           |

| Uplink | rate 1/2                    |                                           |                                           |
| k=64   | 1.32 Mbps @ 2 iters, 69 MHz 0.6% logic, 2% RAM |                                           |                                           |

### Different FPGAs:

<table>
<thead>
<tr>
<th>AR4JA</th>
<th>rate 1/2</th>
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</thead>
<tbody>
<tr>
<td>k=1024</td>
<td>1.6 Mbps @ 14 iters, 57 MHz 5% logic, 22% RAM <strong>XCV1000</strong></td>
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<tr>
<td>Uplink</td>
<td>rate 1/2</td>
</tr>
<tr>
<td>k=64</td>
<td>1.32 Mbps @ 2 iters, 69 MHz 5% logic, 10% RAM <strong>XQR2V1000</strong></td>
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</tbody>
</table>

**Key:**

- **Code:** code rate = k/n
- **k:** bits/clk, syms/clk / iterations = speed
- **FPGA utilization:** %

**Unless otherwise noted:**

- Xilinx Virtex-2 XC2V8000 FPGA
- Average iterations listed are for FER=10^{-5}
- Clock speed is about 80 MHz for all designs
- Stopping rule and buffers allow using average iterations

\[
\text{speed} = \frac{\text{bits/clk}(\text{MHz})}{2(\text{iterations})}
\]
Problem:
LDPC decoders perform best with properly scaled input symbols (like turbo decoders, but unlike Viterbi decoders).

There are many easy solutions:
- This problem has been extensively studied, and solved for turbo decoders.
- The best solution depends on the receiver, and hardware details.

Solution 1: Ask the receiver
- Many radio receivers (such as the DSN) automatically determine signal mean and variance, to improve receiver performance, and for status displays
- Such receivers can scale the symbols for the LDPC decoder

Solution 2: Modify the decoder, so it doesn’t need scaled symbols
- The decoder only needs properly scaled symbols for the min* calculation
- Approximations are available that avoid this requirement
- These approximations cost ~0.2 dB, and simplify the decoder

The math:
Transmit: \( x = \{+1,-1\} \)
Receive: \( y = Ax + \mathcal{N}(0, \sigma^2) \)
Compute LLRs for decoder: \( \lambda = A/\sigma^2 \cdot y \)
This requires an estimate of \( \alpha = A/\sigma^2 \)
Note: \( \text{SNR} = Es/N_0 = A^2/\sigma^2 \), so this is not an SNR estimator, but similar.
Solution 3: Guess that $E_s/N_0 = 2$ dB

- If the guess is right, performance is optimal
- If $E_s/N_0$ is actually smaller, the data is unrecoverable anyway, so nothing is lost
- If $E_s/N_0$ is actually larger, decoder performance isn’t quite as good as it could be, but still better than the design value

Even the ideal performance isn’t good enough here
Performance with guess is better than target BER here

Target BER = $10^{-6}$
Solution 4: Estimate scale from known symbols

- The symbols in the frame sync markers are known (after synchronization)
- Simple estimators can determine the scaling factor from these symbols

Solution 5: Estimate scale from unknown symbols

- There are lots more unknown (coded symbols) than known ones
- Estimators can determine scaling factor from these
- Faster than Solution 4, but more complex

Solution 6: Calibrate for unique receiver behavior

- Some receivers do not produce well distributed soft outputs (such as the IR)
- For these, optimal performance may require pre-calibration of a translation table
- Approximate translation tables may perform nearly as well

The math:
Receive noisy sync symbols \( y \), identify them as \( \hat{x} \). The best scaling factor estimate is:

\[
\hat{\alpha} = \frac{\langle \hat{x} y \rangle_N}{\langle y^2 \rangle_N - \langle (\hat{x} y)^2 \rangle_N}
\]

where \( \langle \cdot \rangle_N \) represents the average of \( N \) observations.

The math:
Solve the simultaneous equations:

\[
2\hat{R} = \langle \alpha y \tanh \hat{\alpha} y \rangle_N
\]
\[
2\hat{R}(2\hat{R} + 1) = \langle \hat{\alpha}^2 y^2 \rangle_N
\]

for \( \hat{R} \) and \( \hat{\alpha} \). Lower complexity approximations exist.

Optimal soft symbol histogram

Measured histogram from Integrated Receiver
Question: How does decoder performance change with a scaling error of $\rho$ dB?

Answer: Under-estimation of the scaling factor by 1 dB degrades the performance about as much as a decrease of $E_b/N_0$ by 0.2 dB; over-estimation has about half that effect.
Conclusions:

- Hard and soft correlators are not good synchronization strategies. Massey published the optimal algorithm in 1972! [But hard correlator is optimal if we just have hard symbols]
- Matching one 64-symbol sync mark isn’t good enough for modern rate-1/2 codes, even with Massey’s optimal algorithm
- Matching two sync marks (128 symbols) is sufficient
- A low-complexity version implemented in FPGA hardware gives the performance shown by the black curve

- Confirmed that current frame marker is appropriate
- No modifications needed to standard, only to decoder/synchronizer implementation
ESTL2 Test Results

ESTL2 Test (Nov. 07, 2007) to verify compatibility with SN hardware

1. The LDPC decoder performs excellently with both the short and medium blocklength LDPC codes.
2. With the pseudo-randomizer, the decoder detected every decoding error.
3. The frame synchronizer performed well in the presence of carrier and symbol slips.
4. The Integrated Receiver performs well with its nonstandard "2%" jitter setting, but there may be problems with tracking Doppler shift. The standard “None” jitter setting limits performance, but LDPC still outperforms RS+CC.
5. The IR’s Viterbi decoder only works with SNR high enough so that BER<10^{-4}. This limits performance of the concatenated RS+CC codes.
Non-Binary LDPC Code C3

Test of a new proposed code

- The decoding complexity of non-binary LDPC codes is currently very high. Further research would be interesting.
- Based on the literature, non-binary LDPC codes may outperform comparable binary LDPC codes.
- Among non-binary LDPC codes, code C3 is not a good candidate
  - High decoding complexity
  - Regular degree distribution sacrifices performance
  - Short blocklength, $k=600$

Performance of several short rate-1/2 codes

- Code C3, regular nonbinary code, $k=600$ bits
- AR4JA code, $k=1024$ bits
- An irregular nonbinary LDPC code, $k=600$ bits
- AR4JA code, $k=512$ bits

Decoding complexity vs. excess $E_b/N_0$

- Irregular nonbinary LDPC code
- CCSDS AR4JA Family
- CCSDS $C_2$
- JPL Proprietary Material
- Outlier, due to error floor of this AR3A code
- Regular degree distribution sacrifices performance
- Large differences in rate and blocksize
- Different families may have different complexity-performance profiles

Andrews, Moision
March 10-14, 2008
Distribution of JPL’s FPGA LDPC Decoder

Industry, NASA centers, and other agencies are using the JPL-designed FPGA LDPC decoders

**Companies**
- Efficient Channel Coding (ECC)
- RTLogic
- Avtec
- L3 Communications
- Lockheed Martin
- Cincinnati Electronics

**NASA centers**
- Johnson Space Center
- Goddard Space Flight Center
- Several JPL projects

**Spacecraft**
- MSL - MRO Proximity Link (implemented; tests ongoing)
- Constellation (baseline plan)
- Cibola Flight Experiment (initial discussions underway)
- AIRSAR (aircraft based)
- MSO (Pre Phase-A)

**LDPC encoders and decoders on FPGA**
- 720 Msps block-circulant LDPC encoder
- 102 Msps decoder for (4096,1/2) AR4JA LDPC code
- 86 Msps decoder for GSFC's r=7/8 C_2 LDPC code
**Infusion Accomplishments**

- **Low-Density Parity-Check (LDPC) code was chosen for all coded links of Constellation**
  - The JPL AR4JA (k = 1024, rate = ½) LDPC code will be used for both uplink and downlink
  - Saves 1.6 dB of power and reduces latency 40 to 90%, compared to legacy code
  - Recommendation based on a comprehensive FEC study (JPL, GSFC, JSC, and led by ITT)
  - Lockheed-Martin has licensed JPL LDPC encoder/decoder technology for CEV spacecraft
  - Choice is contingent on successful TRL advancement from 5 to 9

- **The LDPC code was tested for Space Network (SN) compatibility and performance**
  - LDPC tests conducted 2/20/2007 to 3/2/2007, at JSC Electronic Systems Test Laboratory (ESTL)
  - Decoder operated error-free in all SNR regions the receiver could lock
  - The successful demonstration represents TRL advancement from 4, to 5 (encoder) and 6 (decoder)

- **Mars Science Lab (MSL) to Mars Reconnaissance Orbiter (MRO) link will use same code**
  - Feasibility study for use of AR4JA (1024,½) LDPC code is complete
  - Complete designs for MSL encoder and MRO decoder have been completed

- **TDRS K-Band Upgrade Project (TKUP-A)**
  - Three vendors licensed the JPL LDPC technology during proposal phase
  - Two vendors have been selected to demonstrate LDPC codes: IN-SNEC, and RT Logic
  - Demonstration of AR4JA(1024,1/2) code will occur in Jan. 2008

- **Users of JPL LDPC technology**
  - Cincinnati Electronics, L-3 Space Communications, MIT/LL, Lockheed Martin, RTLogic

- **AOFDM-LDPC system for the Air Force**
CMLP Study

• **Space Planning Working Group (SPWG, formerly SCAWG) Coding, Modulation, and Link Protocol (CMLP) study**
  • **What the study did:**
    - Created extensive catalog of all reasonable modulations and codes
    - Enumerated all communications links in NASA's strategic planning documents
    - Developed comprehensive Figures of Merit by which to compare codes and modulations
    - Created recommendations of codes and modulations for classes of links
  • **CMLP recommendations**
    - Modulations: PCM/PSK/PM, BPSK, QPSK, OQPSK, precoded GMSK, 8-PSK, 16-QAM
    - Codes: CC(7,1/2), RS(255,223), AR4JA LDPC, C2 LDPC
    - All codes and modulations are discussed in CCSDS documents (not all are Blue Books)
  • **Final report completed in September**
## CMLP Study - Recommended Codes

<table>
<thead>
<tr>
<th>Network Parameter</th>
<th>Recommended Technique</th>
<th>Typical Application</th>
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|                   | CCSDS turbo codes (r = 1/6, 1/4, 1/3) | • For low data rate, severely power-constrained links or links which have little spectral containment requirements  
  • Typical application may be a small Mars surface platform with DTE/DFE link |
|                   | CCSDS AR4JA LDPC codes (r = 1/2, 2/3, 4/5) | • Code family with general applicability to most links 
  • Envisioned future replacement to traditional convolutional and concatenated codes 
  • Offers superior coding gain over traditional codes |
|                   | CCSDS C2 LDPC code (r = 7/8) | • For links which are power-constrained and spectrum-constrained 
  • Typical application may be high data rate CAT A mission |
|                   | Convolutional codes | • Mid-Transition: General applicability to most links except spectrum-constrained links 
  • Post-Transition: For severely latency-constrained links only 
  • Offers superior heritage and reliability 
  • Typical application may be a LEO mission’s TT&C link and the high rate science link |
|                   | Legacy Reed-Solomon, BCH | • R-S and BCH have general applicability to most links, especially as outer codes 
  • Need for an outer code is diminished with planned migration to LDPC codes as noted above 
  • Typical application may be a mission which launches prior to the demonstrated operational readiness of LDPC-capable NASA infrastructure |
|                   | Uncoded | • For links which are not power-constrained 
  • Although a mission may not be power constrained, consideration should be given to use of a code because of the benefits to power flux density and resiliency to distortions 
  • Typical application may be an X-band LEO mission downlinking at a very high data rate to the NASA GN |
Latency/Performance Tradeoffs in LDPC codes

Rate 1/2
k = 1024
WER = 10^{-4}

Total # of messages computed, throughout all iterations vs. Decoding Complexity (dB)

15 iterations
ave.

50 iterations
fixed

100 iterations
fixed

Less precoding

AR4JA

G36
Latency/Performance Tradeoffs in LDPC codes

Decreasing WER

Rate 1/2
k = 1024

Decoding Complexity (dB)

Eb/No (dB)

WER=1e-4

G36

AR4JA
# Comparison of Three Proposed Coding System

<table>
<thead>
<tr>
<th></th>
<th>Power Efficiency</th>
<th>Latency (code dimension k)</th>
<th>Complexity /Speed</th>
<th>Patents</th>
<th>CCSDS 'Compatible'</th>
<th>Technology readiness/Infusion</th>
<th>Baseline for Constellation Program</th>
</tr>
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<tbody>
<tr>
<td><strong>LDPC (NASA Orange Book)</strong></td>
<td>&lt;10^{-7} BER, 0.5–1.0 dB imperfection</td>
<td>1/2,...,7/8, 1K,...,16K</td>
<td>Ex: 360 Mbps (4K,1/2) on Xilinx Virtex2 @180MHz</td>
<td>?</td>
<td>Will be royalty free if granted</td>
<td>Orange Book easily converted to Blue Book</td>
<td>Infusion underway for MSL/MRO, tests scheduled for SN</td>
</tr>
<tr>
<td><strong>DVB (CNES)</strong></td>
<td>&lt;10^{-7} BER, 1/4,...,9/10, 16K, 64K</td>
<td>Fast IRA encoder</td>
<td>Large protograph + BCH decoder</td>
<td>?</td>
<td>Codes coupled with modulations and protocol</td>
<td>ASICS for DVB applications</td>
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</tr>
<tr>
<td><strong>SCCC (ESA)</strong></td>
<td>&lt;10^{-7} BER, 0.36–0.90</td>
<td>5876–43740</td>
<td>Fast convolutional encoder</td>
<td>JPL patent plus others</td>
<td>Codes coupled with modulations</td>
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