LDPC Coded Modulation

Preliminary Results on bandwidth efficient coded modulation

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Goal

• To compute the performance of proposed JPL-NASA LDPC codes in the CCSDS Orange Book with high-level Modulations such as OQPSK, 8PSK, and 16QAM (not in CCSDS standard).

• To determine the power and bandwidth efficiency of these codes and compare them with other proposed codes (DVB-S2, SCCC).
Construction Methods

- LDPC coded modulation schemes are constructed by mapping the output of a binary protograph based LDPC codes in the Orange Book to high-level modulation.

- The output of LDPC code is mapped to modulation either:
  1. Directly, or
  2. Through a channel interleaver (so called Bit-interleaved coded modulation (BICM) approach).
Construction Methods (continued)

• For mapping of binary coded bits to signal constellation, distance preserving labeling such as independent Gray labeling has been used.

• A distance preserving labeling means that the signal points are labeled such that the squared Euclidean distance between any two points is lower bounded by the Hamming distance of the corresponding signal labels. This ensures that the minimum squared Euclidean distance will be proportional to the minimum distance of the binary LDPC code.
• Rate 1/2 AR4A LDPC protograph
Bit Interleaved Coded Modulation (BICM) Approach

In this approach a channel interleaver is used between binary encoder and the mapper.
Direct Approach
(without channel interleaver)

- A performance close to the BICM performance can be obtained if the assignment of variable nodes of protograph to the bits of the constellation labels are optimized.
- Thus it is possible to avoid the channel interleaver, however most standards use BICM approach (e.g. DVB-S2, see next page)
"The DVB-S.2 FEC Encoder core provides a complete Forward Error Correction (FEC) encoding solution for DVB-S.2. This core consists of Outer (BCH), Inner (LDPC) encoding and bit-interleaving stages. The bit interleaver supports the interleaving required by all modulation types, which may be QPSK, 8PSK, 16APSK or 32APSK."

Example: DVB-S2 uses BICM approach
High Speed Protograph Decoder

LDPC codes with protograph structure allows very high speed parallel decoder architecture. Independent Gray labeling reduces the complexity of demapper. There is no conflict in memory access. However such conflict may exists in turbo like codes.

**Decoder Speed** = \( \frac{C \times E}{2 \times I} \)

C: Clock speed
E: Expansion factor of base protograph per slice
I: Number of iterations

Example: C=100 MHz
E=128
I=20 (avg)
Decoder Speed=320 Mbps

Fixed I=20 translates to at least 0.2 dB degradation in performance.
Rate-Compatible Code Families

Protograph of AR4A Family with rates 1/2 and higher

<table>
<thead>
<tr>
<th>Code Rate</th>
<th>Protograph Threshold</th>
<th>Capacity</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2</td>
<td>0.560</td>
<td>0.187</td>
<td>0.373</td>
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<tr>
<td>2/3</td>
<td>1.414</td>
<td>1.059</td>
<td>0.355</td>
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<td>3/4</td>
<td>1.980</td>
<td>1.626</td>
<td>0.354</td>
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<td>4/5</td>
<td>2.396</td>
<td>2.040</td>
<td>0.356</td>
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<tr>
<td>5/6</td>
<td>2.717</td>
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<td>6/7</td>
<td>2.980</td>
<td>2.625</td>
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<tr>
<td>7/8</td>
<td>3.197</td>
<td>2.845</td>
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<td>8/9</td>
<td>3.385</td>
<td>3.033</td>
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</table>
Performance of AR4A code family
for input block = 1 kbits

Performance meets the requirements for
FER=10^-4, and FER=10^-6

FPGA Simulations
JPL AR4A Family
solid: BER
dashed: FER

QPSK Modulation

Bit and Frame Error Rate

Eb/No, dB

Rate 1/2
k=1024
Rate 2/3
k=1024
Rate 4/5
k=1024
Rate 5/6
k=1040
Rate 7/8
k=1064
Performance of AR4A code family for input block of 4 kbits (rates < 5/6) and 7kbits (rate 7/8)

Performance meets the requirements for FER=10^{-4}, and FER=10^{-6}
Performance of AR4A code family for input block = 4 kbits

Performance meets the requirements for FER=10^{-4}, and FER=10^{-6}
Bandwidth

While power efficiency can be easily summarized by the single parameter Eb/No representing the SNR per transmitted bit of information, the measure of spectral efficiency is open to several possibilities, as follows:

• **Half-power bandwidth**
  The frequency at which the power spectrum of the signal is 3 dB below its peak value.

• **Equivalent noise bandwidth**
  Defined as
  \[ B_{eq} = \frac{\int_{-\infty}^{\infty} |S(f)|^2 df}{\max_f |S(f)|^2} \]

  where \( S(f) \) is the two-sided power spectral density (PSD). This describes a rectangle of base \( B_{eq} \) and height \( \max_f |S(f)|^2 \) having area equal to the total signal power.

• **Null-to-null bandwidth**
  Representing the width of the main spectral lobe.

• **Fractional power containment bandwidth**
  Also called essential bandwidth. Defined as the bandwidth that contains a given percentage of the signal power.
Some of the possible measures for spectral efficiency: (a) Half-power bandwidth; (b) Null-to-null bandwidth; (c) Equivalent noise bandwidth; (d) Fractional power containment bandwidth.

Here we use the last definition namely fractional power containment bandwidth with 99% or 100% power containment.
Spectral Shaping

• Nyquist square root raised cosine pulse shaping with roll-off factor $\alpha=0.5$, and $\alpha=0.35$ have been recommended in CCSDS standard.

• Spectral efficiency for LDPC coded modulation are computed for 99% and 100% bandwidth definitions, and roll-off factors $\alpha=0$, $\alpha=0.5$, $\alpha=1$. 
Modulation

• The following modulations have been recommended in CCSDS Standard: BPSK, OQPSK, GMSK, FQPSK, and 8PSK.

• QPSK, and 16QAM have not been recommended in CCSDS standard but we provided results for QPSK, and 16QAM.

• OQPSK instead of QPSK is recommended to reduce sidelobe regeneration after nonlinear amplifiers.
Performance of AR4A LDPC coded QPSK Modulation
Compared to theoretical lower bounds for finite block size of 1 kbits

Nyquist roll-off factor = 0

Theoretical lower bound for k=1024 and QPSK FER=10^-4

Unconstrained capacity

FPGA simulated performance for JPL AR4A LDPC coded QPSK FER=10^-4
Performance of AR4A LDPC coded QPSK Modulation
Compared to theoretical lower bounds for finite block size of 4 kbits

Unconstrained capacity
QPSK Capacity
FPGA simulated performance for JPL AR4A LDPC coded QPSK FER=10^-4
Theoretical lower bounds for k=4096 and QPSK FER=10^-4

Spectral Efficiency (bits per sec. per Hz)

Eb/No, dB

0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0

Nyquist roll-off factor = 0

Unconstrained capacity
QPSK Capacity
FPGA simulated performance for JPL AR4A LDPC coded QPSK FER=10^-4
Theoretical lower bounds for k=4096 and QPSK FER=10^-4

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Performance of AR4A LDPC coded 8PSK Modulation Compared to theoretical lower bounds for finite block size of 4 kbits

- Nyquist roll-off factor = 0
- Theoretical lower bounds for $k=4096$ and 8PSK, $FER=10^{-4}$
- FPGA simulated performance for JPL AR4A LDPC coded 8PSK, $FER=10^{-4}$

Spectral Efficiency (bits per sec. per Hz)

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<th>Eb/No, dB</th>
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Power and bandwidth efficiency of TCM, RS/Conv and Constant Envelope Coded Modulation schemes

Eb/No, dB for BER=10^-6
Power and bandwidth efficiency of LDPC Coded Modulation and SCCC Coded Modulation

- ESA’s SCCC degrades at high code rates due to puncturing.
- DVB-S2 degrades for short blocks.
- If the simulations for 8 kbits input block were not available we interpolated the points using theoretical results which provide fairly accurate estimates, provided the simulation results are above error floor region.
- SCCC patent issue
Comparing power and bandwidth efficiency of various coded modulation schemes

\[ \eta = R_b B \text{ (bits/sec/Hz), 99% bandwidth) } \]

\[ \frac{E_b}{N_0} \text{ dB for BER=10}^{-6} \]

- Uncoded
- BPSK
- QPSK
- OQPSK/QPSK
- 4D 8PSK TCM
- FQPSK
- FQPSK turbo
- T-OQPSK+(3,1/2)
- (7,1/2)+RS
- 4D 8PSK TCM α=0.35, 2 bits/Hz
- 16QAM
- 8PSK
- \( k=8192 \)

Other curves and points are also shown for various modulation schemes and error correction techniques.
Conclusion

- A rate-compatible protograph LDPC code family with high-level modulation has been proposed. Circulants on edge of protograph were used to reduce the memory requirement to implement the encoder.
- The proposed JPL’s LDPC coded modulation schemes have near theoretical performance in the waterfall region and error floor compatible with requirements.
- Performance of JPL, ESA, and DVB-S2 codes at BER of $10^{-6}$ are within 0.1 to 0.3 dB. DVB-S2 requires BCH code to lower the error floor with a penalty due to code rate about 0.1 dB.
- In summary we have shown that the LDPC code family in the Orange Book can also support high level modulation for various throughputs with near theoretical performance.